

Description

The ISL54230EVAL2Z, ISL54230EVAL3Z evaluation board is designed to provide a quick and easy method for evaluating the ISL54230 IC.

The ISL54230 IC is a single supply Quad Double-Pole Double Throw (DPDT) analog switch featuring two USB 2.0 Full-Speed/High-Speed compliant switches and two general purpose analog switches. The ISL54230 is designed for applications that require switching, muxing, and/or routing of analog and digital signals. The ISL54230EVAL2Z, ISL54230EVAL3Z evaluation board is developed to evaluate the ISL54230 IC, integrating many features for ease of use in examining the performance of the device under various operating conditions. To help understand the operation of the evaluation board, it is recommended to study the evaluation board schematics found on page 4 of this document and the data sheet for the ISL54230 IC.

The ISL54230 IC is a Quad DPDT analog switch that is operational with a +2.0 to +5.5V supply voltage. The ISL54230 integrates four logic control pins for independent control of each DPDT switch and also includes two output enable pins for disabling certain switches, giving the ISL54230 IC multiple configurations. The evaluation board contains standard BNC connectors, USB Type A and USB Type B connectors to allow the user to easily interface with the IC to evaluate its functions, features, and performance.

This application note will guide the user through the process of configuring and using the evaluation board to evaluate the ISL54230 device.

Key Features

- Quad DPDT Analog Switch for Signal Switching/Muxing/Routing
- Standard BNC Connectors and USB Type A/B connectors
- Convenient Test Points and Connections for Test Equipment
- Manual or External Logic Input Control

Picture of Evaluation Board (Top View)

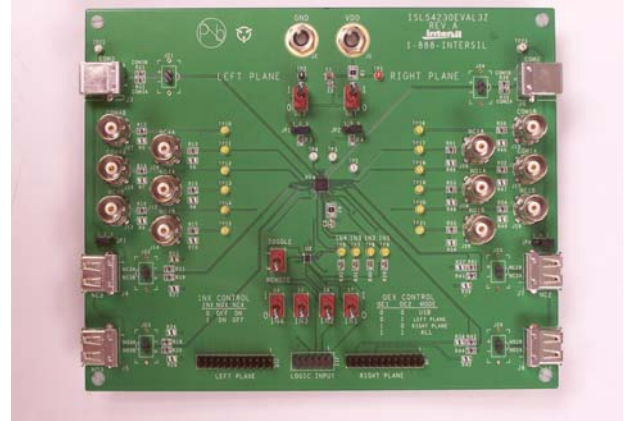


FIGURE 1. ISL540230EVAL2Z, ISL540230EVAL3Z EVALUATION BOARD

Board Architecture/Layout

Basic Layout of Evaluation Board

A picture of the evaluation board is located in Figure 1. For the ISL54230EVAL2Z the ISL54230 IC sits inside the socket located at U1 in the center of the evaluation board. The pin 1 indicator dot of the IC must be aligned with the pin 1 indicator dot inside the socket housing for proper operation. For the ISL54230EVAL3Z, the ISL54230 IC is soldered onto the evaluation board located at the center labeled U1. The evaluation board integrates the necessary connections and components to interface with the ISL54230 for ease of operation.

Note: The ISL54230EVAL2Z and ISL54230EVAL3Z are equivalent evaluation boards except that the ISL54230EVAL2Z uses a socket, while the ISL54230EVAL3Z has the part soldered onto the board to evaluate the IC. In addition, the ISL54230EVAL2Z has toggle switch S3 mislabeled. In the UP position it should be labeled as "TOGGLE" and in the DOWN position it should be labeled as "REMOTE".

Power Supply

The ISL54230 IC requires a supply voltage in the range of +2.0V to +5.5V for proper operation. Banana jacks for VCC (J1) and GND (J2) are located at the top of the board. The evaluation board contains a 4.7μF bulk capacitor, 0.1μF decoupling capacitor and a 0.01μF high frequency local decoupling capacitor at the supply lines.

Logic Control

The evaluation board contains two types of logic control to the digital logic inputs of the ISL54230 IC available to the user. The logic pins can be controlled either through manual (TOGGLE) or external (REMOTE) operation. The logic control pins are manually toggled by the SPDT switches mounted on the evaluation board (S1-S7). When the switch is in the up position (H) the associated logic pin is pulled to V_{DD} for logic HIGH. When the switch is in the down position (L) the associated logic pin is pulled to GND for logic LOW. For manual operation, the jumpers JP1-JP2 need to be in the 1-2 position.

Note: For manual control, leave the toggle switch in the UP position (REMOTE for ISL54230EVAL2Z and TOGGLE for ISL54230EVAL3Z).

For external control via a function generator or switched source, set the jumpers JP1-JP2 in the 2-3 position and place the toggle switch in the DOWN position (TOGGLE for ISL54230EVAL2Z and REMOTE for ISL54230EVAL3Z). This by-passes the S1-S2 and S4-S7 SPDT toggle switches and routes the logic control to the header pin connectors J9-J10 located on the right side of the board. This allows for interfacing a microcontroller or function generator via a ribbon cable connector for remote control.

Note: The logic control pins of the ISL54230 have $1M\Omega$ logic pull down resistors to ground to bias the logic pins to ground when the pins are externally left floating.

Switch Terminals

The evaluation board contains components to interface with all terminals of the Quad DPDT switch. The general purpose analog switches (COM1x and COM4x) are interfaced with BNC connectors. The USB 2.0 compatible switches (COM2x and COM3x) are interfaced with USB Type A/B connectors.

NOTE: All switch terminals can be interfaced to the header pin connectors J9 to J11. Connector J9 interfaces with switches 1 and 2. Connector J10 interfaces with switches 3 and 4. Connector J11 interfaces with the logic control pins OEX and INX. For connecting signals from switch 2 and switch 3 (the signals that are connected to the USB connectors) please see the evaluation board schematic on page 4 for populating the necessary resistor to make the connection.

NOTE: All switch terminals that are interfaced with the standard BNC connectors contain a place holder that can have a surface mount resistor or capacitor placed there. The place holder is connected to the switch terminal on one side and ground on the other side for simulating a resistive or capacitive load. Refer to the evaluation board schematic on page 4 for these place holders.

Power Supply

The DC power supply connected at banana jacks J1 (VDD) and J2 (GND) provides power to the evaluation board. The

evaluation board requires a +2.0V to +5.5V DC power supply for proper operation. The power supply should be capable of delivering $100\mu A$ of current.

Logic Input Voltage

The state of the ISL54230 device is determined by the Truth Table as defined in the ISL54230 data sheet. When in manual operation mode, the logic being toggled by the SPDT switches (S1-S2 and S4-S7) will always drive the voltage of the logic pin to V_{DD} for a HIGH and GND for a LOW. In external control mode, the voltages being driven by an external source must meet appropriate V_{IH} and V_{IL} levels as defined in the data sheet.

The control pins are 1.8V logic compatible up to a +3.3V supply, which allows for control via a standard μ controller.
Logic "0" (LOW) when $\leq 0.5V$
Logic "1" (HIGH) when $\geq 1.4V$

When operating above +3.3V supply, refer to the data sheet for appropriate logic levels to drive the logic pins. It is always recommended to drive the logic pins to the positive supply rail (V_{DD}) and GND to minimize power consumption.

Logic States

INPUT SELECT (INX) PINS

If the INx Pins are logic "HIGH", then the NOx switches are turned ON and the NCx switches are turned OFF. If the INx Pins are logic "LOW", then the NCx switches are turned ON and the NCx switches are turned OFF.

OUTPUT ENABLE (OEX) PINS

The Output Enable pins allow disabling sections of the Quad DPDT switch. Under typical operation, the OE pin should be biased logic "HIGH". This enables all four of the DPDT switches to be active. Refer to the OE Control Truth Table in the data sheet for a list of the possible combinations of switch disable.

USB Connections

USB Type B connectors J3 and J6 connect to the USB host which contains the V_{BUS} power line. USB Type A connectors J4-J5 and J7-J8 connect to a USB device. The V_{BUS} power must be routed to the USB device for proper operation. To prevent both USB devices from receiving V_{BUS} power simultaneously, which may cause connectivity errors, jumpers JP3 and JP4 route power to the USB connectors. When JP3 is in the 1-2 position, V_{BUS} is routed to J5 and when it is in the 2-3 position, V_{BUS} is routed to J4. When JP4 is in the 1-2 position, V_{BUS} is routed to J7 and when it is in the 2-3 position, V_{BUS} is routed to J8.

Note: It is recommended to have the place holders R23, R24, R25-R28, R33, R34, and R37-R40 on the evaluation board unpopulated when sending USB signals through the switches. Failure to do so may result in poor USB signal performance.

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Applications

The ISL54230 is designed to be a Quad DPDT switch for switching, routing, or multiplexing of analog and digital

signals. Such applications include cell phones and PDAs and other personal media devices that may utilize USB2.0/UART/Audio/Power signals.

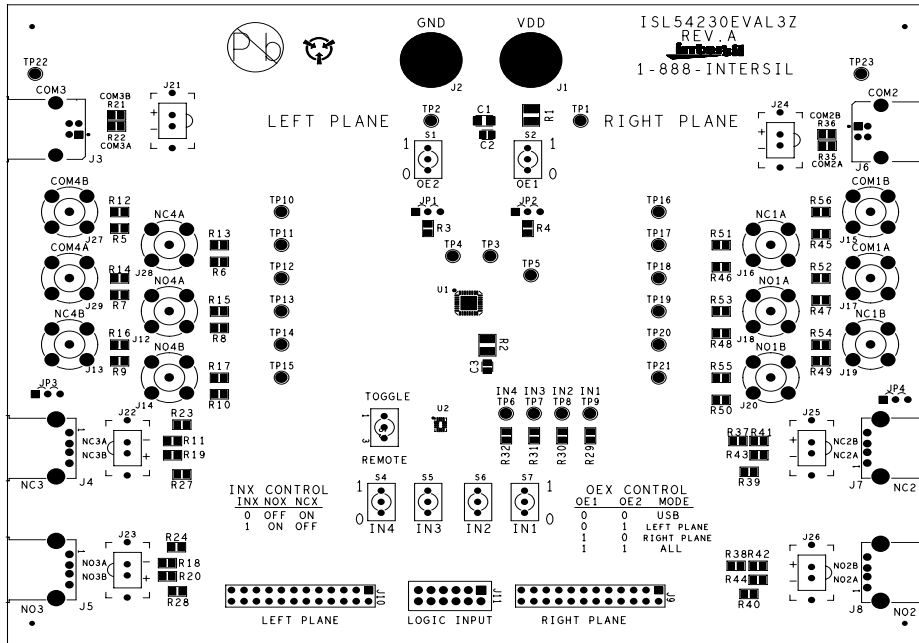


FIGURE 2. ISL54230EVAL3Z TOP VIEW

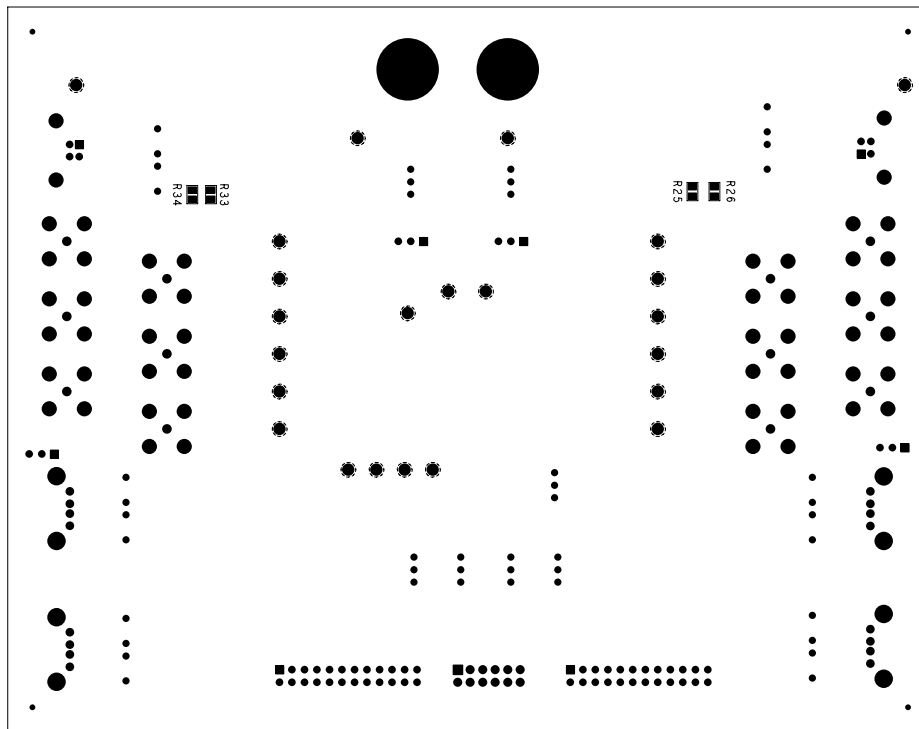


FIGURE 3. ISL54230EVAL3Z BOTTOM VIEW

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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ISL54230EVAL2Z, ISL54230EVAL3Z Evaluation Board Schematic

